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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,913	12/07/2005	Adrianus W.P.G.G. Vaassen	NL03 0686 US1	9556
65913	7590	07/10/2008		
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER DINH, PAUL	
			ART UNIT 2825	PAPER NUMBER
			NOTIFICATION DATE 07/10/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No. 10/559,913	Applicant(s) VAASSEN, ADRIANUS W.P.G.G.	
	Examiner Paul Dinh	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This **SUPPLEMENTAL FINAL** office action is a response to the amendment and remarks filed on 6/27/08.

The remarks are not persuasive, therefore, the rejection based on the previous prior art of record Kuroda are maintained.

Claims 1-10 and newly added claims 11-17 are pending.

Claim Objections

Claims 15-17 are objected to because it is unclear what the Applicant meant by selectively connecting

Claims 15-17 are objected to because the limitations in these claims are not clearly described in the disclosure. See 37 CFR 1.75 (d).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

*A person shall be entitled to a patent unless –
(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by the prior art of record Kuroda (US pub 2001/0039643)

(Claims 1, 7 and similarly recited claim 14)

A power bus (*power supply bus VDD 33 in fig 4*) and a ground bus (*ground bus VSS 32*) for supplying power from respective power and ground pads (*power and ground pads are VDD and VSS terminals/contacts/vias shown in fig 4, slash = and/or*) to a plurality of circuit elements (*circuit elements = i.e., N regions, P region, gates, transistors*) on the IC, characterized in that the power distribution network (as shown in fig 4) comprises a plurality of decoupling cells, wherein the decoupling cells include decoupling capacitors (*decoupling cells include decoupling capacitors are non-logic cells configured as decoupling capacitor shown in fig 6 and implemented in the power*

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distribution network of fig 4, see paragraphs 17-19) for providing a static current flow between the power pad and the ground pad, and wherein the power distribution network is configured such that, for any given circuit element (i.e., one of N regions, P region, gates, transistors in fig 4) on the IC, the combined distance between the power pad and said circuit element, and between the ground pad and said circuit element, is constant

(Fig 4 shows for any given circuit element, i.e., one of N regions, P region, gates, transistors, the combined distance between the power pad (one of: terminal, contact, via that connected to VDD bus 33) and said circuit element, and between the ground pad (one of: terminal, contact, via that connected to VSS bus) and said circuit element, is constant (constant due to and/or in terms of one or more of the following reasons:

- a. Symmetrical layout as shown in fig 4, i.e., 32 and 33, 30d and 31e, and symmetrical layout of terminal, contact, via connecting 30d and 31e*
 - b. Same/identical lengths/layout as shown in fig 4, i.e., 32 and 33, 30d and 31e*
 - c. Complementary layout, as shown in fig 4, of the busses (32, 33), terminals/pads (30d, 31e)*
 - d. Diagonally opposite corners layout, as shown in fig 4, of the terminals/pads (30d, 31e) and vias/contacts (pads) that connected to 32-33 and 30d, 31e*
- (Note that claims 2-3 in the instant application recited power pad and the ground pad are arranged complementary and at diagonally opposite corners of the IC, this is clearly disclosed by the prior art fig 4, and further more, the same/identical lengths/layout in a symmetrical manner as shown in fig 4, i.e., 32 and 33, 30d and 31e, further equivalently suggest the constant combined distance as claimed.)*

(Claims 2-10) wherein the power distribution network is configured such that, as the distance of any given circuit element from the power pad increases, the distance from the ground pad decreases in a complementary manner (fig 4); wherein the power pad and the ground pad are arranged at diagonally opposite corners of the IC (fig 4); wherein the power distribution network comprises: a power bus comprising a vertical section connected to the power pad and one or more horizontal sections connected to the vertical section (fig 4); a ground bus comprising a vertical section connected to the ground pad and one or more horizontal sections connected to the vertical section (fig 4); wherein the vertical section of the power bus is arranged parallel to the vertical section of the ground bus, such that the one or more horizontal sections of the power bus interleave the one or more horizontal sections of the ground bus (fig 4); wherein a horizontal section of the power bus and a horizontal section of a ground bus form a row

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for powering one or more of the circuit elements (fig 4); wherein one or more circuit elements are located between the horizontal section of the power bus and the horizontal section of the ground bus (fig 3-4); wherein the decoupling cells are configured to be the same height as the circuit elements (fig 3-4, 6); wherein the decoupling cells are arranged between circuit elements on the IC (fig 3, 6); wherein the power distribution network comprises one or more smaller-power distribution networks having the same configuration (fig 3-4, 6).

(Claims 11-13) wherein the power distribution network maintains the voltage drop between the power pad and each circuit element constant.

(Fig 4 shows the power distribution network maintains the voltage drop between the power pad and each circuit element constant due to and/or in terms of one or more of the following reasons:

- a. *Symmetrical layout as shown in fig 4, i.e., 32 and 33, 30d and 31e, and symmetrical layout of terminal, contact, via connecting 30d and 31e*
- b. *Same/identical lengths/layout as shown in fig 4, i.e., 32 and 33, 30d and 31e*
- c. *Complementary layout, as shown in fig 4, of the busses (32, 33), terminals/pads (30d, 31e)*
- d. *Diagonally opposite corners layout, as shown in fig 4, of the terminals/pads (30d, 31e) and vias/contacts (pads) that connected to 32-33 and 30d, 31e*
(Note that claims 2-3 in the instant application recited power pad and the ground pad are arranged complementary and at diagonally opposite corners of the IC, this is clearly disclosed by the prior art fig 4, and further more, the same/identical lengths/layout in a symmetrical manner as shown in fig 4, i.e., 32 and 33, 30d and 31e, further equivalently suggest the constant combined distance as claimed)

wherein the decoupling cells maintain the voltage drop between the power pad and each circuit element constant (due to symmetrical, identical, opposite corner layout and similar length as shown in fig 4, 6) wherein the decoupling cells selectively couple each of said given circuit elements to maintain combined distance constant (as explained above with respect to fig 4, 6)

(Claims 15-17) wherein the decoupling cells maintain the constant combined distance for a circuit element by selectively connecting the conductors to the circuit element to decrease/increase the distance between the circuit element and one of the power pad and the ground pad in a manner that is complementary to an increased/decreased distance between the circuit element and the other one of the power pad and the ground pad *(as detailed above, fig 4, 6 show power pad and ground pad in a*

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complementary manner that maintained the combined distance constant with respect to circuit elements as detailed above) wherein the decoupling cells (in fig 6) maintain a static current between the power pad and the ground pad by selectively connecting the circuit elements via the conductors (fig 4-6).

Response to Applicant Remarks

The prior art of record discloses all the elements recited in the claims as detailed above.

Correspondence Information

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/

Primary Examiner, Art Unit 2825